IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Michael B. Galles, et al.
Serial No.:	10/696,146
Filing Date:	October 29, 2003
Confirmation No.:	5506
Group Art Unit:	2181
Examiner:	William M. Treat
Title:	MULTI-PROCESSOR SYSTEM AND METHOD OF ACCESSING DATA THEREIN

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

REPLY BRIEF

Applicant has appealed to the Board of Patent Appeals and Interferences from the Official Action reopening prosecution issued May 12, 2010 rejecting Claims 1-20. Applicant respectfully submitted a Notice of Appeal on August 12, 2010 and an appeal brief on January 12, 2011. In response to the Examiner's Answer issued March 17, 2011, Applicant respectfully submits herewith their brief in reply.

REMARKS

As explained in more detail below, the Examiner's rejections of these claims cannot be properly maintained. Appellant respectfully requests the Board to reverse these rejections and instruct the Examiner to issue a Notice of Allowance with respect to these claims.

The Examiner's Answer dated March 17, 2011 consists of substantially identical arguments to those presented in the Office Action reopening prosecution issued May 12, 2010, along with brief additional comments for each issue responding to Appellant's arguments presented in the Appeal Brief. To reduce the burden on the Board, Appellant specifically addresses only the comments of the Examiner's Answer directed to Appellant's arguments in the Appeal Brief. The remaining portions of the Examiner's Answer have already been addressed in Appellant's Appeal Brief. The headings below follow the headings of the Appeal Brief.

1. Claims 1-10 and 16-20 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite.

In the Examiner's Answer, the Examiner repeats verbatim the statements from the last Office Action. These statements have been addressed in the Appeal Brief. The only additional comment provided by the Examiner is that Applicant indicated that the changes were minor and clearly supported by FIGURE 2 though the legends on the original drawings and the description in the original specification do not make clear this support. As provided in the drawings, CPU 20 is part of processor 12 as shown in FIGURE 1 along with memory 16 integrated therewith in processor 12. As clearly shown in FIGURE 2, an expanded view of CPU 20 is provided. CPU 20 is shown with an integrated memory directory 18 and an integrated

memory controller 30. No changes have been made to the drawings. The global reference to processor 12 in the original specification does not change what is clearly shown in FIGURE 2 of the CPU 20 with an integrated memory directory 18 and an integrated memory controller 30. Thus, the claims are fully supported by the drawings and the specification. Therefore, the claims are in compliance with 35 U.S.C. §112, second paragraph.

2. Claims 1-20 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite.

In the Examiner's Answer, the Examiner takes the position that the term 'integrated' has no meaning whatsoever and could be disregarded completely. However, the term is being used and there is no unusual meaning of the term 'integrated' being applied. The term 'integrated' is used only to describe that the elements are not separate from each other. It is clearly shown in FIGURE 2 that memory directory 18 and memory controller 30 are a part of CPU 20 and not separate therefrom. Thus, within CPU 20 are a memory directory 18 and a memory controller 30. As shown in FIGURE 1, CPU 20 and memory 16 are a part of processor 12 and not separate therefrom. Thus, within processor 12 are a memory 16 and the CPU 20. As a result, memory controller 30 and memory directory 18 are not just in the same room or on the same board as CPU 20 but are within and a part of CPU 20 and thus integrated therein in the normal sense of the word. Similarly, CPU 20 and memory 16 are not just in the same room or on the same board as processor 12 but are within and a part of processor 12 and thus integrated therein in the normal sense of the word. Therefore, the claims are in compliance with 35 U.S.C. §112, second paragraph.

3. Claims 1-10 and 16-20 stand rejected under 35 U.S.C. §112, first paragraph, for containing subject matter not described in the specification.

In the Examiner's Answer, the Examiner merely repeats verbatim the statements provided in the last Office Action. Applicant has already addressed these statements in the Appeal Brief.

4. Amendments made to the specification stand objected to under 35 U.S.C. §132(a) as introducing new matter.

In the Examiner's Answer, the Examiner merely repeats verbatim the statements provided in the last Office Action. Applicant has already addressed these statements in the Appeal Brief.

5. The drawings stand objected under 37 C.F.R. §1.84(p)(5) for including reference signs not mentioned in the specification.

In the Examiner's Answer, the Examiner repeats verbatim the statements provided in the last Office Action. These statements have been addressed in the Appeal Brief. The only additional comment provided by the Examiner is that the changes made to the specification would be inconsistent in scope with the patented parent application's drawings and the Examiner's arguments. However, there are no changes being made to the drawings. The drawings in the present Application are identical to the drawings in the parent application. Moreover, the claims in the present Application are directed to a different inventive aspect than the claims granted in the parent application. Further, the changes made to the specification in this Application are consistent with the drawings and were made in as minimal of form to not require

changes to the drawings or add subject matter to the Application in order address the Examiner's identified inconsistencies and confusion thereof. Therefore, Applicant respectfully submits that the drawings are in compliance with 37 C.F.R. §1.84(p)(5).

6. Claims 11-15 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,890,217 issued to Kabemoto, et al.

In the Examiner's Answer, the Examiner states that Applicants arguments are irrelevant since they are not directed to the embodiment of the Kabemoto, et al. patent with only one CPU per processor module. FIGURE 2 of the Kabemoto, et al. patent merely shows how processing modules 10-1 to 10-5 are interconnected by system buses 12-1 and 12-2. As clearly shown and described in the Kabemoto, et al. patent, a processing module 10-1 may have at least one processing element 14-1 though four processing elements 14-1 to 14-4 are shown as an example in FIGURE 3. A processing element 14-1 has a processor (CPU) 16-1, a cache unit 18-1, and a snoop unit 20-1. See col. 16, lines 10-21, of the Kabemoto, et al. patent. Even if a processing module 10-1 has only one processing element 14-1 with a separate processor 16-1 with CPU 34, cache unit 18-1, and snoop unit 20-1 as shown in FIGURE 4, the Kabemoto, et al. patent fails to show that its processor 16-1 with CPU 34 has an integrated memory directory or an integrated memory controller as required by the claimed invention. In fact, the directory memory 30 of the Kabemoto, et al. patent is not only separate and apart from its processing element 14-1 and processor 16-1 with CPU 34 but cannot directly communicate with its processing element 14-1 and processor 16-1 with CPU 34 as the directory memory 30 is

associated with a separate memory control module 25. The same implementation applies in the Kabemoto, et al. patent with its local memory 28 which is separate and apart from its processor 16-1. Thus, the Kabemoto, et al. patent fails to disclose having its local memory 28 integrated within its processor 16-1 nor does the Kabemoto, et al. patent disclose having its memory directory integrated with its central processing unit 34 of its processor 16-1 as required by the claimed invention. Moreover, because of this, the Kabemoto, et al. patent has no capability to maintain a memory reference in a memory directory integrated with a central processing unit to information in a different processor as required by the claimed invention. Therefore, Applicant respectfully submits that Claims 11-15 are not anticipated by the Kabemoto, et al. patent.

7. Claims 1-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,374,331 issued to Janakiraman, et al.

In the Examiner's Answer, the Janakiraman, et al. patent, as pointed out by the Examiner, discloses integrating memory 2510 on the processor chip 2500 and integrating the memory controller 2520 on the processor chip 2500. See col. 8, lines 11-15, of the Janakiraman, et al. patent. It seems that the Examiner has no problems with the use of the term 'integrating' as provided in the Janakiraman, et al. patent. However, the Janakiraman, et al. patent fails to disclose that such integration of the memory controller 2520 is with the core processor 2540 as memory controller 2520 is associated with memory 2510 and separate and apart from core processor 2540. Moreover, there is still no memory directory in the core processor 2540 of the Janakiraman, et al. patent let

alone on its processor chip 2500. The Janakiraman, et al. patent clearly shows a coherency controller 6000 and a coherency directory 6030 external to the processor chip 2500. In fact, processor chips 2500 and 3500 of the Janakiraman, et al. patent connect to and share coherency controller 6000 and coherency directory 6030. Moreover, the Janakiraman, et al. patent teaches away from integrating the coherency controller on the processor chip. See col. 8, lines 29-35, of the Janakiraman, et al. patent. The Examiner provided no rebuttal in the Examiner's Answer to this point. To further show that the Examiner's justification for rejecting the claims as obvious are without merit, the Examiner equates the coherency controller 6000 and the coherency directory 6030 of the Janakiraman, et al. patent as the external switch and external directory in rejecting Claim 1 and as such could not be also integrated into the processor chip. Thus, one of skill in the art would hardly recognize from the Janakiraman, et al. patent an implementation where the memory directory would be integrated with a central processing unit of a processor as required by the claimed invention. Therefore, Applicant respectfully submits that Claims 1-20 are patentably distinct from the Janakiraman, et al. patent.

8. Claims 2, 3, 18, and 20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,374,331 issued to Janakiraman, et al. in view of the Gupta paper.

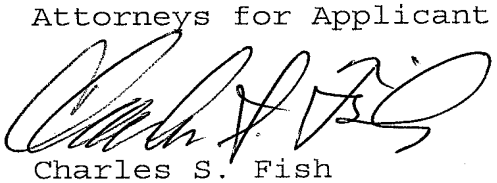
In the Examiner's Answer, the Examiner merely repeats verbatim the statements provided in the last Office Action. Applicant has already addressed these statements in the Appeal Brief.

CONCLUSION

Applicant has clearly demonstrated that the present invention as claimed is clearly distinguishable over all the art cited of record, either alone or in combination, and satisfies all requirements under 35 U.S.C. §§101, 102, and 103, and 112. Therefore, Applicant respectfully requests the Board of Patent Appeals and Interferences to reverse the rejection of the Examiner and instruct the Examiner to issue a Notice of Allowance of all pending claims.

The Commissioner is hereby authorized to charge any fees or credit any overpayments associated with this Application to Deposit Account No. 02-0384 of BAKER BOTTS L.L.P.

Respectfully submitted,
BAKER BOTTS L.L.P.
Attorneys for Applicant



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